Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A semiconductor integrated circuit comprising:

a plurality of DRAM CIRCUITS;

a control circuit that receives a test control signal to perform a test control in which said plurality of RAM circuits are tested while the access to said plurality of DRAM circuits is subsequently changed for each row and said plurality of DRAM circuits are cyclically accessed for each row;

an input selector that is controlled by said control circuit and inputs a DRAM macro signal to said plurality of DRAM circuits at the time of a test; and

an output selector that is controlled by said control circuit, and outputs output signals of said plurality of DRAM circuits sequentially to a macro output terminal at the time of the test.

2. (original) A semiconductor integrated circuit according to claim 1, wherein said control circuit is directly connected to a control signal input terminal to be controlled from said control signal input terminal and thereby the control circuit is directly controlled from said control signal input terminal.

3. (original) A semiconductor integrated circuit according to claim 1, wherein said input selector that is controlled by said control circuit to input a DRAM macro signal to one of said plurality of DRAM circuits at the time of a normal operation.

4. (original) A semiconductor integrated circuit according to claim 3, wherein said control circuit is directly connected to a control signal input terminal to be controlled from said control signal input terminal and thereby the control circuit is directly controlled from said control signal input terminal.

5. (original) A semiconductor integrated circuit according to claim 1, wherein said output selector is controlled by said control circuit to output an output signal of one of said plurality of DRAM circuits to the macro output terminal at the time of a normal operation.

6. (original) A semiconductor integrated circuit according to claim 5, wherein said control circuit is directly connected to said control signal input terminal to be directly controlled from said control signal input terminal and thereby is controlled directly from said control signal input terminal.

7. (original) A semiconductor integrated circuit according to claim 1, wherein said control circuit performs a test control of said plurality of DRAM circuits in such a manner that the access to first rows of said plurality of DRAM circuits is performed while successively changing the access to said plurality of DRAM circuits, and, following the access to the first rows of said plurality of DRAM circuits, the same access as that to the first rows of said plurality of DRAM circuits is performed from the next rows to the last rows of said plurality of DRAM circuits while successively changing the access to said plurality of DRAM circuits for each row.

8. (original) A semiconductor integrated circuit according to claim 7, wherein said control circuit is connected directly to said control signal input terminal to be directly controlled from the control signal input terminal and

thereby the control circuit is directly controlled from said control signal input terminal.

9-14. (cancelled)

15. (currently amended) A semiconductor integrated circuit ~~according to claim 9,~~ comprising:

a plurality of DRAM circuits;

a plurality of control circuits each of which is provided corresponding to one of said plurality of DRAM circuits, and receives a test control signal to perform a test control of said corresponding one DRAM circuit; and

an output selector that is controlled by said control signal, and outputs output signals of said plurality of DRAM circuits sequentially to a macro output terminal at the time of a test,

wherein said control circuits performs a test control of said plurality of DRAM circuits in such a manner that the access to first rows of said plurality of DRAM circuits is performed while successively changing the access to said plurality of DRAM circuits, and, following the access to the first rows of said plurality of DRAM circuits, the same access as that to the first rows of said plurality of DRAM circuits is performed from the next rows to the last rows of said plurality of DRAM circuits while successively changing the access to said plurality of DRAM circuits for each row.

16. (original) A semiconductor integrated circuit according to claim 15, wherein said control circuits are directly connected to a control signal

input terminal to be controlled from said control signal input terminal and thereby the control circuits are directly controlled from said control signal input terminal.

17. (cancelled).

18. (currently amended) A semiconductor integrated circuit ~~according to claim 17,~~ comprising:

a plurality of DRAM circuits;

a control circuit that receives a control signal and controls said plurality of DRAM circuits simultaneously and independently from each other;

an input selector for supplying a DRAM macro signal input to one of said plurality of DRAM circuits; and

an output selector that selects an output signal of one of said plurality of DRAM circuits and outputs the output signal to a macro output terminal,

wherein on receiving the control signal, said control circuit controls said plurality of DRAM circuits so that data is read from said plurality of DRAM circuits sequentially and transferred to the outside of the DRAM circuits.

19. (original) A semiconductor integrated circuit according to claim 18, wherein said control circuit supplies the bank active signal BACT to one of said plurality of DRAM circuits and then controls said output selector in a manner such that said output selector selects the output signal of said one DRAM circuit, and then, after the data is read and outputted from columns of said one DRAM circuit sequentially, supplies a bit line precharge signal BPRC to said one DRAM circuit, and

said control circuit supplies the bank active signal BACT to another DRAM circuit while supplying a read signal READ to said one DRAM circuit, and controls said output selector so as to select the output signal of said another DRAM circuit while supplying the bit line precharge signal BPRC to said one DRAM circuit.